

## Patent claims

1. A method for producing a binary information memory cell,
  - 5 • in which a first electrically conductive region is produced in and/or on a substrate;
  - in which an auxiliary structure of a prescribed thickness is produced on the first electrically conductive region,
  - 10 • in which a second electrically conductive region is produced on the auxiliary structure,
  - in which the auxiliary structure is removed after the second electrically conductive region has been produced, so that a cavity is formed between the
  - 15 first electrically conductive region and the second electrically conductive region, the distance between the first electrically conductive region and the second electrically conductive region corresponding to a tunnel spacing;
  - 20 • in which the first and second electrically conductive regions are set up such that upon application
    - of a first voltage to the electrically conductive regions a structure which at least
    - 25 partially bridges the distance between the electrically conductive regions is formed from material from at least one of the electrically conductive regions;
    - of a second voltage to the electrically
    - 30 conductive regions material from a structure which at least partially bridges the distance between the electrically conductive regions is taken back.
- 35 2. The method as claimed in claim 1,  
in which the auxiliary structure used is a self-assembled monolayer.

3. The method as claimed in claim 1,  
in which the auxiliary structure is produced using an  
atomic layer deposition method.
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4. The method as claimed in claim 1,  
in which the auxiliary structure is produced using a  
molecular beam epitaxy method.
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5. The method as claimed in one of claims 1 to 4,  
in which the prescribed distance is between  
approximately 0.5 nm and approximately 5 nm.
6. The method as claimed in one of claims 1 to 5,  
15 in which the prescribed distance is between  
approximately 0.6 nm and approximately 2 nm.
7. The method as claimed in one of claims 1 to 6,  
in which the first electrically conductive region is a  
20 first interconnect and the second electrically  
conductive region is a second interconnect, which  
interconnects are produced so as to run toward one  
another essentially at right angles.
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8. The method as claimed in one of claims 1 to 7,  
in which the substrate used is a silicon substrate.
9. The method as claimed in one of claims 1 to 8,  
in which the first electrically conductive region or  
30 the second electrically conductive region are formed  
from
- a solid-state electrolyte,
  - a glass comprising metal ions
  - a semiconductor comprising metal ions; or
  - 35 • a chalcogenide.
10. The method as claimed in one of claims 1 to 9,

in which the first electrically conductive region or the second electrically conductive region are formed from silver sulfide.

- 5 11. The method as claimed in one of claims 1 to 10,  
in which the first electrically conductive region or  
the second electrically conductive region are formed  
from metal material.
- 10 12. The method as claimed in one of claims 1 to 11,  
in which the first electrically conductive region or  
the second electrically conductive region are formed  
from
- silver;
  - 15 • copper;
  - aluminum;
  - gold and/or
  - platinum.